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FORM

APR 13 2007

(to be used for all correspondence after initial filing)

Application Number	10/516,583
Filing Date	March 24, 2005
First Named Inventor	Charles Eugene Stroud
Art Unit	2863
Examiner Name	Demetrius R. Pretlow
Attorney Docket Number	46872-308797

## ENCLOSURES (check all that apply)

- |  |   |  |
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| <input type="checkbox"/> Fee Transmittal Form<br><input checked="" type="checkbox"/> Fee Attached<br><input type="checkbox"/> Amendment / Reply<br><input type="checkbox"/> After Final<br><input type="checkbox"/> Affidavits/declaration(s)<br><input type="checkbox"/> Extension of Time Request<br><input type="checkbox"/> Express Abandonment Request<br><input checked="" type="checkbox"/> Information Disclosure Statement<br><input type="checkbox"/> Certified Copy of Priority Document(s)<br><input type="checkbox"/> Reply to Missing Parts/<br>Incomplete Application<br><input type="checkbox"/> Reply to Missing Parts<br>under 37 CFR 1.52 or 1.53 | <input type="checkbox"/> Drawing(s)<br><input type="checkbox"/> Licensing-related Papers<br><input type="checkbox"/> Petition<br><input type="checkbox"/> Petition to Convert to a<br>Provisional Application<br><input type="checkbox"/> Power of Attorney, Revocation<br>Change of Correspondence Address<br><input type="checkbox"/> Terminal Disclaimer<br><input type="checkbox"/> Request for Refund<br><input type="checkbox"/> CD, Number of CD(s) ____<br><input type="checkbox"/> Landscape Table on CD | <input type="checkbox"/> After Allowance Communication to TC<br><input type="checkbox"/> Appeal Communication to Board<br>of Appeals and Interferences<br><input type="checkbox"/> Appeal Communication to TC<br>(Appeal Notice, Brief, Reply Brief)<br><input type="checkbox"/> Proprietary Information<br><input type="checkbox"/> Status Letter<br><input checked="" type="checkbox"/> Other Enclosure(s)<br>(please identify below):<br>Express Mail Certificate;<br>PTO/SB/08a with 31 references;<br>23 Non-US patent references;<br>Credit Card Form PTO-2038 for \$180 (IDS<br>Fee); and<br>Return Postcard. |
|--|---|--|

Remarks

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Kilpatrick Stockton LLP

Signature

Printed Name

John C. Alemanni

Date

April 13, 2007

Reg. No.

47,384

## CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

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Typed or printed name

Date

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



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Attorney Docket No. 46872-308797  
PATENT

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Charles Eugene Stroud, et al. Art Unit: 2863  
Appl. No.: 10/516,583  
Filed: 3/24/2005 Examiner: Demetrius R. Pretlow  
For: Method For Delay-Fault Testing In Field – Programmable  
Gate Arrays

INFORMATION DISCLOSURE STATEMENT  
(SUBMISSION AFTER FILING OF AN APPLICATION  
BUT BEFORE FINAL REJECTION OR NOTICE OF ALLOWANCE  
OR CONCURRENTLY WITH A RULE 1.114 RCE APPLICATION)

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO/SB/08A(s), attached hereto.

II. COPIES (check at least one box)

- a. ☐ This application was filed before June 30, 2003. Accordingly, submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

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- b. ☒ This application was filed on or after June 30, 2003. Accordingly, copies of cited U.S. patents and patent application publications therefore are not included. Copies of foreign patent documents and non-patent literature are included.
- c. ☐ Some or all of the documents listed on the PTO/SB/08A are not enclosed because they were cited in the International Search Report and copies should already be in the PTO file. If copies are needed, please contact the undersigned.

III. CONCISE EXPLANATION OF THE RELEVANCE  
(check at least one box)

- a. ☒ **DOCUMENTS IN THE ENGLISH LANGUAGE**

The patents, publications, or other information listed on the attached PTO/SB/08A are in the English language and therefore, do not require a statement of relevancy.

- b. ☐ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

- c. ☐ **ENGLISH LANGUAGE SEARCH REPORT**

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

- d. ☐ **OTHER**

The following additional information is provided for the Examiner's consideration.

FEES

IV. ☐ THIS IDS IS BEING FILED UNDER 37 C.F.R. § 1.97(b):  
(check one box)

- a. ☐ within three months of the filing date of a national application (37 C.F.R. § 1.97(b)(1)). No fee or statement is required. *(This section is not to be used with RCE's.)*
- b. ☐ within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or statement is required.
- c. ☐ concurrently with the filing of a Request for Continued Examination under § 1.114 (37 C.F.R. § 1.97(b)(4)). No fee or statement is required.
- d. ☐ before the mailing date of a first Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or statement is required.  
In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) below, or, if no statement has been made, charge our deposit account in the amount of \$180.00 as required by 37 C.F.R. § 1.17(p).

V. ☒ THIS IDS IS BEING FILED UNDER 37 C.F.R. § 1.97(c):  
(check one box)

before the mailing date of a Final Office Action under 37 C.F.R. § 1.113 (See 37 C.F.R. § 1.97(c)(1)) or before the mailing date of a Notice of Allowance under 37 C.F.R. § 1.311 (See 37 C.F.R. § 1.97(c)(2)).

- a. ☒ No statement; therefore, a fee in the amount of \$180.00 as required by 37 C.F.R. § 1.17(p).
- or
- b. ☐ See the statement below. No fee is required.

VI. STATEMENT UNDER 37 C.F.R. § 1.97(e) (check only one box)

The undersigned hereby states that

- a. ☐ each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS; or
- b. ☐ no item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the IDS.
- c. ☐ Some of the items of information were cited in a communication from a foreign Patent Office. As to this information, the undersigned states that each item of information contained in the IDS was first cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby states that no item of this remaining information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application and, to the best of my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement.

VII. PAYMENT OF FEES (check one box)

- ☒ Credit Card Form PTO-2038 in the amount of \$180 is enclosed for the above-identified fee.
- ☐ Please charge Deposit Account No. 16-1435 in the amount required by 37 C.F.R. § 1.17(p) for the above-indicated fee. A triplicate copy of this paper is attached.
- ☐ No fee is required.

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Attorney Docket No. 46872-308797  
PATENT

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 16-1435.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 16-1435 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

KILPATRICK STOCKTON LLP

Date: April 13, 2007

By: 

John C. Alemanni

1001 West Fourth Street  
Winston-Salem, NC 27101-2400

Attachment(s): ☒ PTO/SB/08A  
☒ Documents  
☐ Foreign Search Report  
☒ Fee  
☐ Other:



Substitute for form 1449B/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Sheet 2 of 3

**Complete if Known**

Application Number	10/516,583
Filing Date	March 24, 2005
First Named Inventor	Charles Eugene Stroud
Art Unit	2863
Examiner Name	Demetrius R. Pretlow
Attorney Docket Number	46872-308797

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	9.	ABRAMOVICI, M. et al., "Self-Test for FPGAS and CPLDs Requires No Overhead," Electronic Design, 1997, pp.121-128.	
	10.	ABRAMOVICI, M. et al., "Using Roving STARS for On-Line Testing and Diagnosis of FPGAs for Fault Tolerant Applications," Proc. IEEE International Test Conf., 1999, pp.973-982.	
	11.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Diagnosis of FPGA Logic Blocks," Proc. IEEE International Test Conf., 1997, pp.539-547.	
	12.	ABRAMOVICI, M. et al., "Improving BIST-Based Diagnosis for Roving STARS," Proc. IEEE International On-Line Testing Symp., 2000, pp.31-39.	
	13.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Test and Diagnosis of FPGA Logic Blocks," IEEE Transactions on Very Large Scale Integration Systems, 2001, 9(1):159-172.	
	14.	ABRAMOVICI, M. et al., "Roving STARS: An Integrated Approach to On-Line Testing, Diagnosis, and Fault Tolerance for FPGAs in Adaptive Computing Systems," Proc. NASA/DoD Evolvable Hardware Conf., 2001, pp.73-92.	
	15.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Delay Fault Testing in FPGAs," Proc. IEEE International On-Line Testing Symp., 2002, pp.131-134.	
	16.	ABRAMOVICI, M. et al., "Using Embedded FPGAs for SoC Yield Enhancement," Proc. ACM/IEEE Design Automation Conf., 2002, pp.713-724.	
	17.	ABRAMOVICI, M. and C. STROUD, "BIST-Based Delay Fault Testing in Field Programmable Gate Arrays," J. Electronic Testing: Theory & Applications, 2003, 19(5):549-558.	
	18.	ABRAMOVICI, M. et al., "On-Line Built-In Self Test and Diagnosis of FPGA Logic Resources," IEEE Trans. On VLSI Systems, 2004, 12(12):1284-1294.	
	19.	CHEMLAR, E., "FPGA Interconnect Delay Fault Testing," Proc. Int'l Test Conf., 2003, pp.1239-1247.	
	20.	EMMERT, J. et al., "Dynamic Fault Tolerance in FPGAs via Partial Reconfiguration," Proc. IEEE International Symp. On Field-programmable Custom Computing Machines, 2000, pp.165-174.	

Examiner  
SignatureDate  
Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet 3 of 3

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First Named Inventor	Charles Eugene Stroud
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	21.	EMMERT, J. et al., "Predicting Performance Penalty for Fault Tolerance in Roving Self-Testing Areas (STARs)," Proc. International Conf. On Field Programmable Logic, 2000, pp.545-554.	
	22.	EMMERT, J. et al., "On-Line Fault Tolerance for FPGA Interconnect with Roving STARs," Proc. IEEE International Symp. On Defect and Fault Tolerance in VLSI Systems, 2001, pp.445-454.	
	23.	STROUD, C. et al., "Built-in Self-Test of Logic Blocks in FPGAs," Proc. IEEE VLSI Test Symp., 1996, pp.387-392.	
	24.	STROUD, C. et al., "Evaluation of FPGA Resources for Built-In Self-Test of Programmable Logic Blocks," Proc. ACM International Symp. On Field Programmable Gate Arrays, 1996, pp.107-113.	
	25.	STROUD, C. et al., "Selecting Built-In Self-Test Configurations for Field Programmable Gate Arrays," Proc. IEEE Automatic Test Conf., 1996, pp.29-35.	
	26.	STROUD, C. et al., "Using ILA Testing for BIST in FPGAs," Proc. IEEE International Test Conf., 1996, pp.68-75.	
	27.	STROUD, C. et al., "BIST-Based Diagnostics of FPGA Logic Blocks," Proc. IEEE International Test Conf., 1997, pp.539-547.	
	28.	STROUD, C. et al., "Built-In Self-Test of FPGA Interconnect," Proc. IEEE International Test Conf., 1998, pp.404-411.	
	29.	STROUD, C. et al., "On-Line BIST and Diagnosis of FPGA Interconnect Using Roving STARs," Proc. IEEE International On-Line Test Symp., 2001, pp.27-33.	
	30.	STROUD, C. et al., "BIST-Based Diagnosis of FPGA Interconnect," Proc. IEEE International Test Conf., 2002, pp.618-627.	
	31.	SMITH, J. et al., "An Automated BIST Architecture for Testing and Diagnosing FPGA Interconnect Faults," J. Electronic Testing: Theory & Applications, 2006, 22(4):239-253.	

Examiner  
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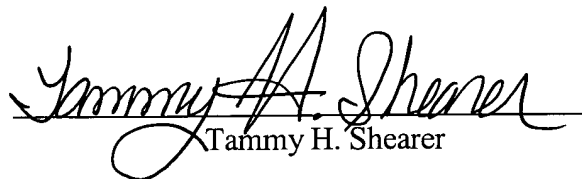
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Serial No. : 10/516,583

Filing Date : March 24, 2005

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Tammy H. Shearer